EP93xx Silicon Rev E
Design Guidelines

1. Introduction

This document is intended to inform customers using EP93xx Rev E0/E1/E2 devices in their designs of certain important considerations. The recommendations contained in this document are lesser-known requirements of the EP93xx devices. Unless otherwise noted, these guidelines apply for all EP93xx Rev E devices.

This document should be used in conjuction with the particular EP93xx device data sheet and/or user's guide.

2. Real Time Clock (RTC)

A real time clock (RTC) signal is required to be connected to the EP93xx device. This clock is used by internal logic to boot the device. The EP93xx device will not power up if there is no connection to the EP93xx RTC clock pin(s).

3. RTC External Oscillator Circuit

An external RTC oscillator circuit is required to ensure proper EP93xx power-up and RTC time tracking accuracy. The circuit must provide a clean, symmetrical square wave. For the recommended RTC circuit design, please refer to AN265, which can be found at:
http://www.cirrus.com/en/pubs/appNote/AN265REV2.pdf

4. External Memory Configuration

A problem exists when performing a *Sync* boot (ADSO=1 when reset is released) with the 32-bit EP93xx device using 16-bit Flash memory and 32-bit SDRAM connected to SDCS3.

The EP93xx devices were originally designed to support booting from Synchronous Flash devices such as the AT49LD3200 or the MT28S4M16LCTG-10. These Sync Flash devices were designed to be accessed by an SDRAM controller. They behaved like SDRAM but were actually Flash devices. If one of these Sync Flash devices was used, it was intended to be connected to SDCS3. That way, the boot configuration would apply the boot memory width to SDCS3. These Sync Flash devices that the EP93xx device was originally designed to use are no longer produced. The EP93xx devices do not support the newer Sync Flash devices like the K3 product offered from Intel Corporation.

The EP93xx device latches the state of ASD0 and nCS[7:6] upon reset, along with several other signals. If ASD0 is sampled high, Sync boot mode is selected. The EP93xx swaps the address map for nCS0 with nSDCS3. Bits nCS[7:6] specify the data bus width of the boot memory device. Refer the appropriate EP93xx User's Guide for more detail on boot modes.

If the EP93xx device is configured for Sync boot mode as described above, the EP93xx device will force SDCS3 to be 16 bits wide. Software can not reprogram SDCS3 to be 32 bits wide.

To avoid this situation, configure the EP93xx device to boot in the Async mode. Refer to the Appropriate EP93xx User's Guide for details about the memory map for Sync and Async modes. Refer to the ARM920T Core and Advanced High Speed Bus (AHB) chapters.

Another way to avoid this situation is to use an SDRAM chip select other than SDCS3, when in Sync Boot mode.

5. Default Static Memory Wait State

When the EP93xx device is configured for internal boot mode, it first executes the on-chip boot ROM after reset. The boot ROM sets the Static Memory Controller (SMC) registers with a wait state value that may be suitable for faster Flash memory devices, such as the Intel Strata Flash, but this value may not be suitable for other slower Flash devices.

EP93xx users that plan to use slower Flash devices are advised to configure the EP93xx for external boot mode so that the boot ROM is bypassed. The hardware default wait state value for external boot mode is set to its maximum to accommodate slow Flash devices.

6. 2x SSP (Synchronous Serial Port) Clock – Revision E2 only

The hard-coded divide-by-2 block in the SSP (also called SPI™) clock input path was removed for Rev E2. This change increases the upper and lower operating range by a factor of 2. The maximum SPI clock rate of 3.6864 MHz is now increased by 2x to 7.3728MHz.

The deletion of the hard coded divide by 2 block will require those using SSP to adjust the SSPCPSR or the SSPCR0 register divider value if the external device can not accommodate the increased SSP clock rate automatically.

If a mixture of revisions are used, then the CHIP_ID register can be used to identify the silicon revision and adjust the SSP registers accordingly. The CHIP_ID register, bits 31:28, identifies the silicon revision. The silicon revision is decoded as follows:

        0000 - Rev A
        0001 - Rev B
        0010 - Rev C
        0011 - Rev D0
        0100 - Rev D1
        0101 - Rev E0
        0110 - Rev E1
        0111 - Rev E2

If SSP is not being used, or the external SPI device can automatically accommodate the 2x clock increase, then no software modifications are required.

7. Boot Mode Pin Latching

An issue exists where boot mode pins may not properly latch a logic zero when RSTOn de-asserts. Boot mode pins that may exhibit this issue are: CSn7, CSn6, CSn2 and CSn1. The other boot mode pins are not affected.

Boot mode pins are latched on the rising edge of RSTOn. This pin is open collector and may have slow rise times, depending on the value of the external pull up resistor connected to this pin. The boot mode pins require a 5ns minimum hold time after RSTOn is de-asserted. If the timing is not met, boot mode pins intended to be latched as a logic zero may be latched as a logic one.

To prevent this issue, the following is recommended:

 - To reduce rise time to approximately 200 ns maximum, place a 1k pull up resistor on RSTOn.
 - Place a small capacitor on the required boot mode signal to delay the signal from rising too quickly after RSTOn is released. The value of the capacitor is dependant on the system design. A capacitor in the range of 100-220pF is recommended. This is only required for pins that need to be latched as a logic zero. Refer to the following diagram.
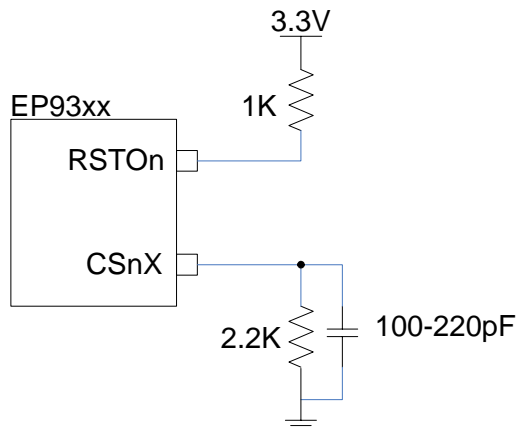
Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com**